D8

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :		(11) International Publication Number:
H01L 27/12	A1	WO 96/34415
		(43) International Publication Date: 31 October 1996 (31.10.96)

(21) International Application Number: PCT/US96/04620

(22) International Filing Date: 3 April 1996 (03.04.96)

(30) Priority Data:
08/430,997 28 April 1995 (28.04.95) US

(71) Applicant: NATIONAL SEMICONDUCTOR CORPORATION [US/US]; M/S D3-579, 1090 Kifer Road, Sunnyvale, CA 94086-3737 (US).

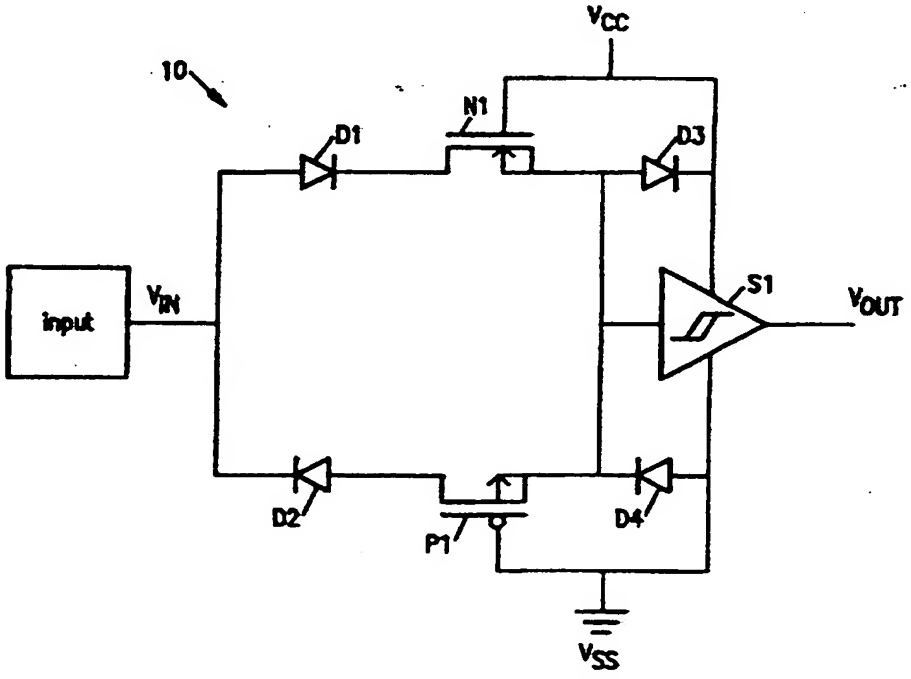
(72) Inventor: MERRILL, Richards, B.; 258 Alta Vista, Daily City, CA 94014 (US).

(74) Agent: CONSER, Eugene; National Semiconductor Corporation, M/S D3-579, 1090 Kifer Road, Sunnyvale, CA 94086-3737 (US).

(81) Designated States: DE, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: CMOS INTERFACE CIRCUIT FORMED IN SILICON-ON-INSULATOR SUBSTRATE



(57) Abstract

A CMOS circuit formed in a silicon-on-insulator (SOI) substrate includes MOSFETs having drain and body diffusions which extend through the silicon layer to the surface of the insulating layer. Each of drains of the N-channel and P-channel MOSFETs serves also as a terminal (anode or cathode) of a diode that is connected in series with the MOSFET. This structure allows the CMOS device to be fabricated as a completely symmetrical structure without adding processing steps beyond those customary in fabricating conventional CMOS devices.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

CMOS INTERFACE CIRCUIT FORMED IN SILICON-ON-INSULATOR SUBSTRATE

Richard Billings Merrill

FIELD OF THE INVENTION

This invention relates to interface circuits and, in particular, to an interface circuit formed in a silicon-on-insulator substrate that is capable of converting a high-voltage signal to a low-voltage signal.

BACKGROUND OF THE INVENTION

Silicon-on-insulator (SOI) substrates are generally fabricated by forming a SiO_2 layer on the surface of a silicon "bond wafer" and bonding the bond wafer to a base wafer to form an $Si-SiO_2-Si$ sandwich. The bond wafer is then ground and polished until a layer of silicon of a desired thickness is formed. The resulting structure is a sandwich consisting of a relatively thick silicon layer (sometimes referred to as the "handle wafer") which is overlain by relatively thin layers of SiO_2 and silicon. Semiconductor devices are typically formed in the top silicon layer.

Until now, SOI substrates have not found wide acceptance, and most integrated circuits have been formed in a silicon substrate or in an epitaxial layer formed on the surface of a silicon substrate. CMOS circuits, for example, are normally fabricated by first creating a well that is doped to a conductivity type that is opposite to the conductivity type of the silicon substrate. A P-well is formed, for example, in an N-type substrate, with the NMOS device being formed in the P-well and the PMOS device being formed in the N-type substrate. The CMOS device is normally isolated from other devices in the substrate by, for example, surrounding the CMOS device with a field oxide region.

This structure presents several problems. First, since one of the MOSFETs is formed in a well while the other is formed in the substrate, the CMOS device as a whole cannot be symmetrical. Second, forming a diode in the well creates a parasitic bipolar transistor, with the substrate acting as the collector. Therefore, practically all of the current through the diode will be diverted into the substrate. Third, forming the field oxide requires additional processing steps.

These drawbacks are overcome in the CMOS interface circuit of this invention.

SUMMARY OF THE INVENTION

The circuit of this invention includes a CMOS device that is formed in an SOI substrate. The N-channel MOSFET includes a body diffusion of P-type material which extends to the insulating layer of the SOI substrate. The N-type source of the NMOSFET is formed within the body diffusion, and the N-type drain is formed as a separate diffusion adjacent the body diffusion. The source and drain are separated by a channel region near the surface of the substrate, and a gate is formed over the channel region. The drain of the NMOSFET also serves as the cathode of a diode which has as its anode an adjacent P-type diffusion.

Conversely, The P-channel MOSFET includes a body diffusion of N-type material which likewise extends to the insulating layer of the SOI substrate. The P-type source of the NMOSFET is formed within the body diffusion, and the P-type drain is formed as a separate diffusion adjacent the body diffusion. The source and drain are separated by a channel region near the surface of the substrate, and a gate is formed over the channel region. The drain of the PMOSFET also serves as the anode of a diode which has as its cathode an adjacent N-type diffusion.

The diffusions are electrically isolated from each other because (except for the sources, which are surrounded by the body diffusions) each diffusion extends to the insulating layer.

This structure may advantageously be used to create an interface circuit which draws no current and which is capable of converting a high-voltage signal to a low-voltage signal. The input terminal, which receives the high-voltage signal, is connected in common to the anode of the diode that is associated with the NMOSFET and the cathode of the diode that is associated with the PMOSFET. The MOSFETs are used as pass transistors which provide intermediate outputs at their respective source terminals. These intermediate outputs may be directed to a Schmitt trigger if a binary output is desired.

The interface circuit is symmetrical and may be fabricated with no processing steps beyond those ordinarily used in making a CMOS device. The need for special isolating structures such as field oxide regions is eliminated.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a circuit diagram of a zero current, high voltage interface circuit in accordance with the invention.

Fig. 2 illustrates a plan view of an integrated embodiment of the circuit shown in Fig. 1.

Fig. 3 illustrates a cross-sectional view of the integrated embodiment shown in Fig. 2 taken at section III-III.

Figs. 4A-4F illustrate steps of a process that may be used to fabricate the integrated circuit embodiment illustrated in Figs. 2 and 3.

DESCRIPTION OF THE INVENTION

Fig. 1 illustrates a circuit diagram of a CMOS interface circuit 10 formed on a silicon-on-insulator substrate which is capable of transforming a high voltage input signal to a low voltage output signal while drawing essentially no input current.

A high-voltage input signal V_{IN} is delivered to the anode of a diode D1 and the cathode of a diode D2. Diode D1 is connected in a series path with an N-channel MOSFET N1 and a diode D3, the gate of MOSFET N1 being connected to a positive supply voltage V_{CC}. Diode D2 is connected in a second series path with a P-channel MOSFET P1 and a diode D4, the gate of MOSFET P1 being connected to a negative supply voltage V_{SS} (in this case ground). The source terminals of MOSFETS N1 and P1 are connected to the inputs of a Schmitt trigger S1, which delivers a low-voltage output signal V_{OUT}.

For purposes of explanation, it is assumed that V_{IN} oscillates between +30 V and -30 V. When V_{IN} goes high, diode D2 is reverse-biased, blocking the signal from MOSFET P1. Diode D2 is forward-biased and delivers a voltage 30 V - V_{bc} ~ 29 V to the drain of MOSFET N1. MOSFET N1 acts as a pass transistor. Assuming that V_{CC} = 3.3 V, the source of MOSFET N1 will charge up to a level $V_{GS} - V_{TN}$, or about 2.6 V, and will draw essentially no current. Schmitt trigger S1 may, for example, be designed to deliver a V_{OUT} of 3.3 V when its input is high. Diode D3 protects the input of Schmitt trigger S1 from an overvoltage condition. The voltage at the input of Schmitt trigger S1 is clamped to V_{CC} + V_{bc}.

When V_{IN} goes low, diode D1 is reverse-biased and diode D2 delivers a voltage -30 V + V_{bc} ~ -29 V to the drain of MOSFET P1, which also acts as a pass transistor. The source of MOSFET P1 charges to a voltage V_{TP} ~ 0.7 V, drawing essentially no current, and

V_{TP} is therefore delivered to the input of Schmitt trigger S1. In this situation Schmitt trigger S1 might deliver a V_{OUT} of 0 V, for example. Diode D4 protects the input of Schmitt trigger against an undervoltage condition by clamping it to $-V_{be}$.

Schmitt trigger S1 is of conventional CMOS design.

In accordance with this invention, interface circuit 10 is fabricated in integrated form on a silicon-on-insulator (SOI) substrate. Fig. 2 shows a plan view of a SOI substrate 20, and Fig. 3 shows a cross-sectional view of the substrate taken at section III-III of Fig. 2.

Referring initially to Fig. 3, substrate 20 contains a handle wafer 31, a silicon dioxide layer 32 and a silicon layer 33. Silicon layer 33 has a thickness which is preferably in the range 1-2 μm. SOI substrates suitable for use with this invention are available, for example, from Shin-Etsu Handotai Co., Ltd., 1-4-2 Marunouchi, Chiyoda-ku, Tokyo, 100, Japan.

Fig. 2 illustrates that circuit 10 is formed of two large wells 21 and 22 that are formed in substrate 20. As described below, diode D1 and MOSFET N1 are formed in well 21, and diode D2 and MOSFET P1 are formed in well 22.

As is evident from Fig. 2, wells 21 and 22 each contain a series of annular diffusions or wells which are shown in cross-section in Fig. 3. Starting at the periphery of well 21, a lightly doped N- well 200 serves to isolate well 21 laterally from other devices formed in substrate 20. Inside of N- well 200 are a P- well 201 and an N- well 202 which form the anode and cathode, respectively, of diode D1. A P+ contact diffusion 201C (not shown in Fig. 2) is formed in P- well 201 and provides a contact for a line 34 which carries V_{IN}.

N- well 202 also serves as the drain of MOSFET N1. A central P- well 203 forms the body of MOSFET N1 and includes a P+ contact diffusion 203C. A relatively shallow N+ well 204 surrounds contact diffusion 203C and serves as the source of MOSFET N1. A polysilicon gate 205 is formed above the surface of silicon layer 33 and is separated by a gate oxide layer from a channel region of P- well 203. Owing to the presence of gate 205, P- well 203 is not visible in the plan view of Fig. 2.

The gate oxide layer and other features above the surface of silicon layer 33, such as metal and passivation layers, are not shown in Fig. 3 in the interests of clarity. These structures are formed by techniques well known in the art.

Starting at the periphery of well 22, a lightly doped P- well 206 serves to isolate well 22 laterally from other devices formed in substrate 20. Inside of P- well 206 are a N- well 207 and an P- well 208 which form the cathode and anode, respectively, of diode D2. An N+ contact diffusion 207C (not shown in Fig. 2) is formed in N- well 207 and provides a contact for line 34.

P- well 208 also serves as the drain of MOSFET P1. A central N- well 209 forms the body of MOSFET P1 and includes an N+ contact diffusion 209C. A relatively shallow P+ well 210 surrounds contact diffusion 209C and serves as the source of MOSFET P1. A polysilicon gate 211 is formed above the surface of silicon layer 33 and is separated by a gate oxide layer from a channel region of N- well 209. Owing to the presence of gate 211, N- well 209 is not visible in the plan view of Fig. 2.

Line 34, which carries V_{IN}, is connected to P- well 201 (the anode of diode D1) via contact diffusion 201C and to N- well 207 (the cathode of diode D2) via

contact diffusion 207C. V_{CC} is connected to gate 205, and V_{SS} (ground) is connected to gate 211. P+ diffusion 203C and N+ well 204 (the body contact and source, respectively, of MOSFET N1) are shorted together and are connected to the anode of diode D3 and the input of Schmitt trigger S1. N+ diffusion 209C and P+ well 210 (the body contact and source, respectively, of MOSFET P1) are shorted together and are connected to the cathode of diode D4 and the input of Schmitt trigger S1. Diodes D3 and D4 and Schmitt trigger S1 can be formed in substrate 20 or externally by methods that are well known in the art.

Since the bottoms of wells 200-203 and 206-209 are adjacent the top surface of insulating silicon dioxide layer 32, each of these wells is isolated from other regions of silicon layer 33. Neither N-channel MOSFET N1 nor P-channel MOSFET P1 is formed in a well which is of opposite conductivity from the substrate, as with conventional CMOS devices. As a result, MOSFETs N1 and P1 are completely symmetrical.

Figs. 4A-4F illustrate a conventional CMOS process sequence that can be used to fabricate an interface circuit of the kind shown in Figs. 2 and 3. The process begins with substrate 20, which as noted above includes handle wafer 31, silicon dioxide layer 32 and silicon layer 33. As shown in Fig. 4A, a pad oxide layer 400 is deposited to a thickness of about 450 Å, followed by a nitride layer 401 (1350 Å) and a resist layer 402. Pad oxide layer 400 and nitride layer 401 are patterned and etched and N-type dopant is implanted, preferably phosphorus.

This produces the N-wells as shown in Fig. 4B. Resist layer 402 is then stripped, and a selective oxide layer 403 is grown to a thickness of about 5000 Å over the N-wells.

As shown in Fig. 4C, nitride layer is removed, and P-type dopant is implanted, preferably boron flouride. The resulting P-wells are shown in Fig. 4D.

Selective oxide layer 403 is then etched back, and the N- and P-wells are driven in at a temperature of 1100° for two hours. The remaining oxide is then stripped, and a gate oxide layer 404 is grown on the top surface of silicon layer 33. A polysilicon layer 405 is deposited on gate oxide layer 404 and doped with phosphorus. Polysilicon layer 405 and gate oxide layer 404 are then masked and etched, forming gates 205 and 211 as shown in Fig. 4D. An N+ blocking mask 406 is deposited and patterned, and N-type dopant is implanted at a concentration of about $2x10^{12}$ cm^{-2}.

This forms the N+ regions shown in Fig. 4E. N+ blocking mask 406 is removed, and a P+ blocking mask 407 is laid down and patterned. P-type dopant is implanted at a concentration of about $2x10^{12}$ cm^{-2}, yielding the structure shown in Fig. 4F.

It will be understood by those skilled in the art the known steps may be included in the process for such purposes as forming field oxide regions, providing lightly doped drains (e.g., using gate spacers), and adjusting the threshold voltage of the MOSFETs.

Following the formation of the doped regions within silicon layer 33, metal and insulating layers are deposited over the substrate to properly connect MOSFETs N1 and P1 and diodes D1 and D2 to diodes D3 and D4 and Schmitt trigger S1. Methods of making these connections and of fabricating diodes D1 and D2 and Schmitt trigger S1 in CMOS are well known in the art.

The embodiment described above is illustrative only and not limiting. It will be apparent to those skilled in the art that numerous alternative embodiments may be constructed in accordance with the broad principles of this invention.

CLAIMS

I claim:

1. A CMOS device formed in a silicon-on-insulator (SOI) substrate, said CMOS device comprising:

an N-channel MOSFET comprising a first N well, a first P well and a relatively shallow N diffusion within said first P well, a portion of said first P well adjacent a surface of said SOI substrate forming a channel of said N-channel MOSFET, said first N well and said first P well extending to a surface of an insulating layer within said SOI substrate, a first gate being formed over said channel of said N-channel MOSFET; and

a P-channel MOSFET comprising a second P well, a second N well and a relatively shallow P diffusion within said second N well, a portion of said second N well adjacent a surface of said SOI substrate forming a channel of said P-channel MOSFET, said second P well and said second N well extending to said surface of said insulating layer, a second gate being formed over said channel of said P-channel MOSFET.

2. The CMOS device of Claim 1 further comprising a third P well formed in said SOI substrate adjacent said first N well and a third N well formed in said SOI substrate adjacent said second P well.

3. The CMOS device of Claim 2 wherein said first N well and said third P well together form a first diode and said second P well and said third N well together form a second diode, said first and second diodes being coupled to an input signal.

4. The CMOS device of Claim 2 wherein said first gate is connected to a first voltage and said second gate is connected to a second voltage.

5. The CMOS device of Claim 2 wherein said first P well and said second N well are connected to an input of a Schmitt trigger.

6. The CMOS device of Claim 5 wherein said first P well is shorted to said relatively shallow N diffusion, and said second N well is shorted to said relatively shallow P diffusion.

7. The CMOS device of Claim 5 further comprising a third diode connected between said input of said Schmitt trigger and said first voltage, and a fourth diode connected between said input of said Schmitt trigger and said second voltage.

8. A method of fabricating a CMOS interface circuit, said method comprising:

providing a silicon-on-insulator substrate, said substrate comprising a silicon layer;

introducing N-type dopant into said silicon layer so as to form first and second N-wells;

introducing P-type dopant into said silicon layer so as to form first and second P-wells adjacent said first and second N-wells, respectively;

introducing N-type dopant into said silicon layer so as to form a relatively shallow N diffusion within said first P-well;

introducing P-type dopant into said silicon layer so as to form a relatively shallow P diffusion within said second N-well; and

forming a first gate over a channel region within said first P-well and forming a second gate over said second N-well,

wherein said first and second N-wells and said first and second P-wells extend to an interface between said silicon layer and an insulating layer of said substrate.

9. The method of Claim 8 further comprising the steps of introducing P-type dopant into said silicon layer so as to form a third P-well adjacent said first N-well and introducing N-type dopant into said silicon layer so as to form a third N-well adjacent said second P-well.

10. The method of Claim 9 further comprising connecting said third P-well and said third N-well to an input signal.

11. The method of Claim 9 further comprising connecting said first P-well and said second N-well to an input of a Schmitt trigger.

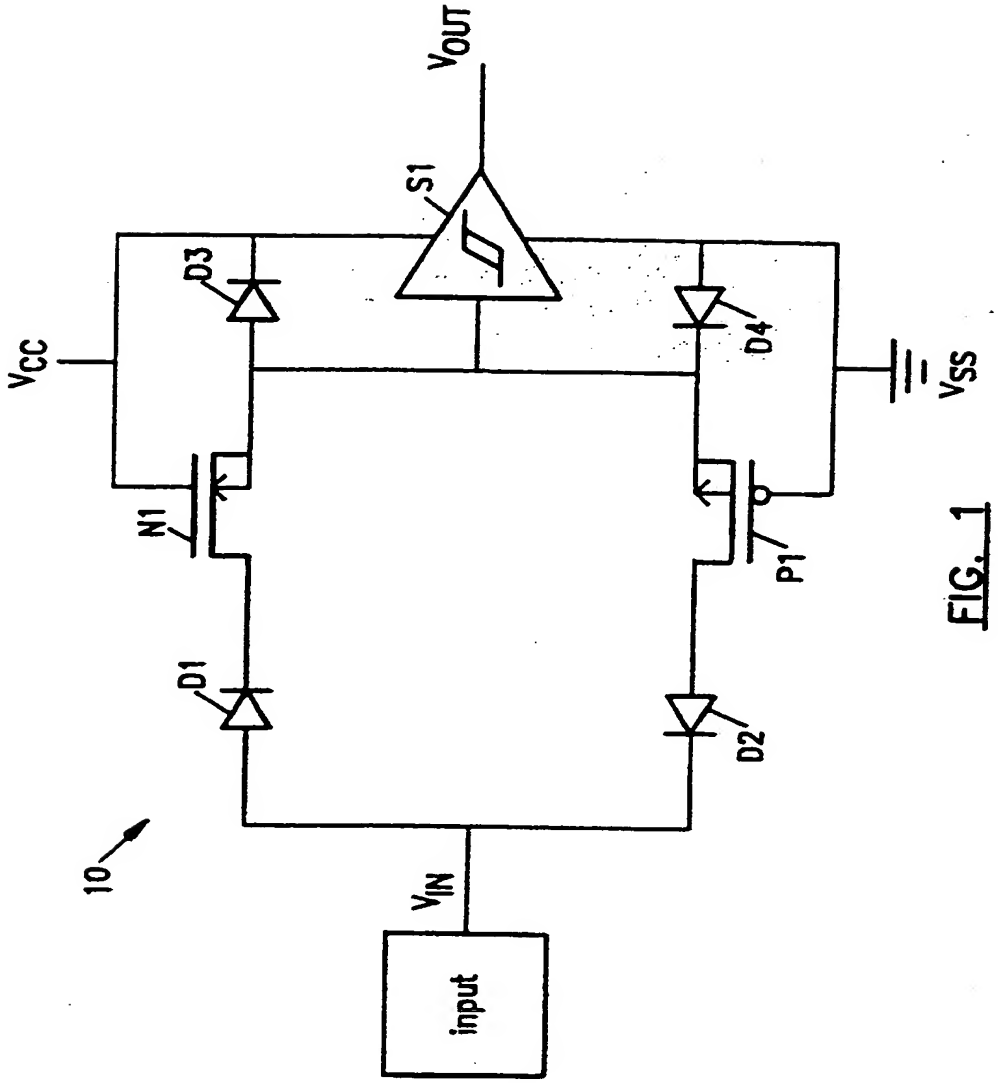


FIG. 1

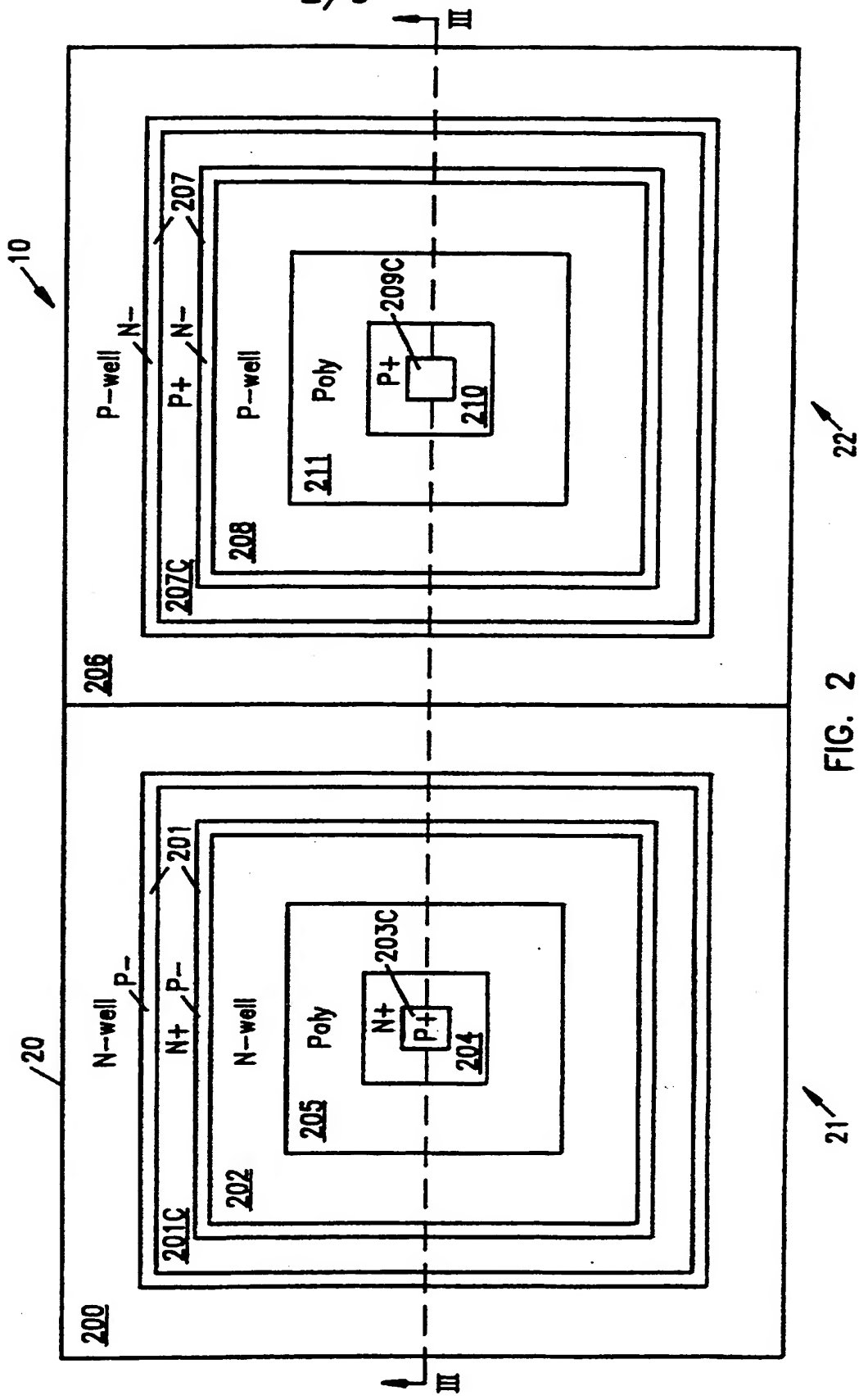

III
10
207
N-
P-well
N-
P+
P-well
Poly
209C
P+
210
211
208
207C
206
22
201
P-
N-well
P-
N+
N-well
Poly
203C
N+
P+
204
205
202
201C
200
20
21
III

FIG. 2

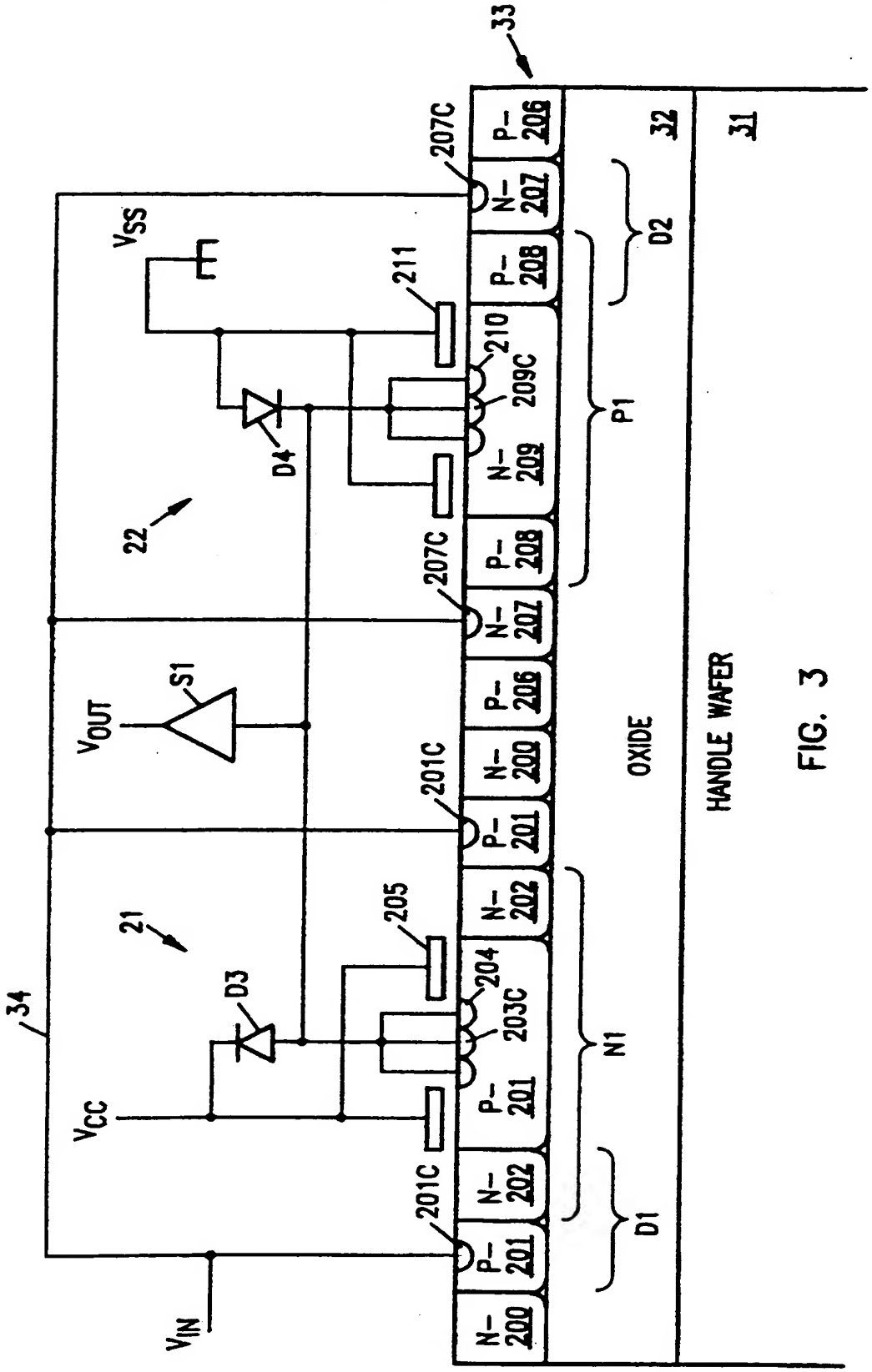

33
207C
P- 206
N- 207
P- 208
211
210
209C
N- 209
P- 208
N- 207
P- 206
N- 200
P- 201
N- 202
205
204
203C
P- 201
N- 202
P- 201
N- 200
V_{SS}
D4
22
V_{OUT}
S1
21
D3
V_{CC}
V_{IN}
34
P1
D2
N1
D1
32
31
OXIDE
HANDLE WAFER

FIG. 3

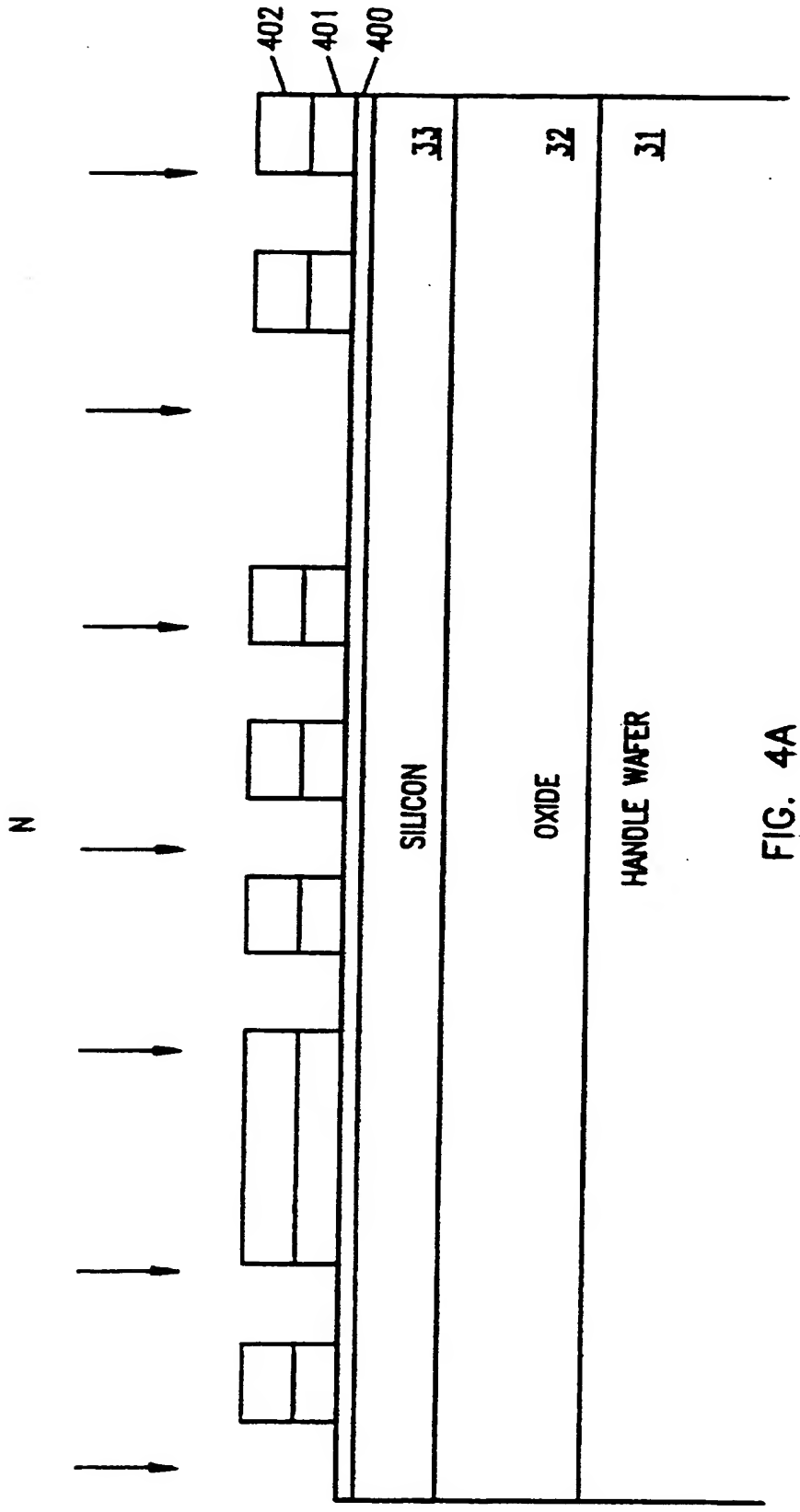


FIG. 4A

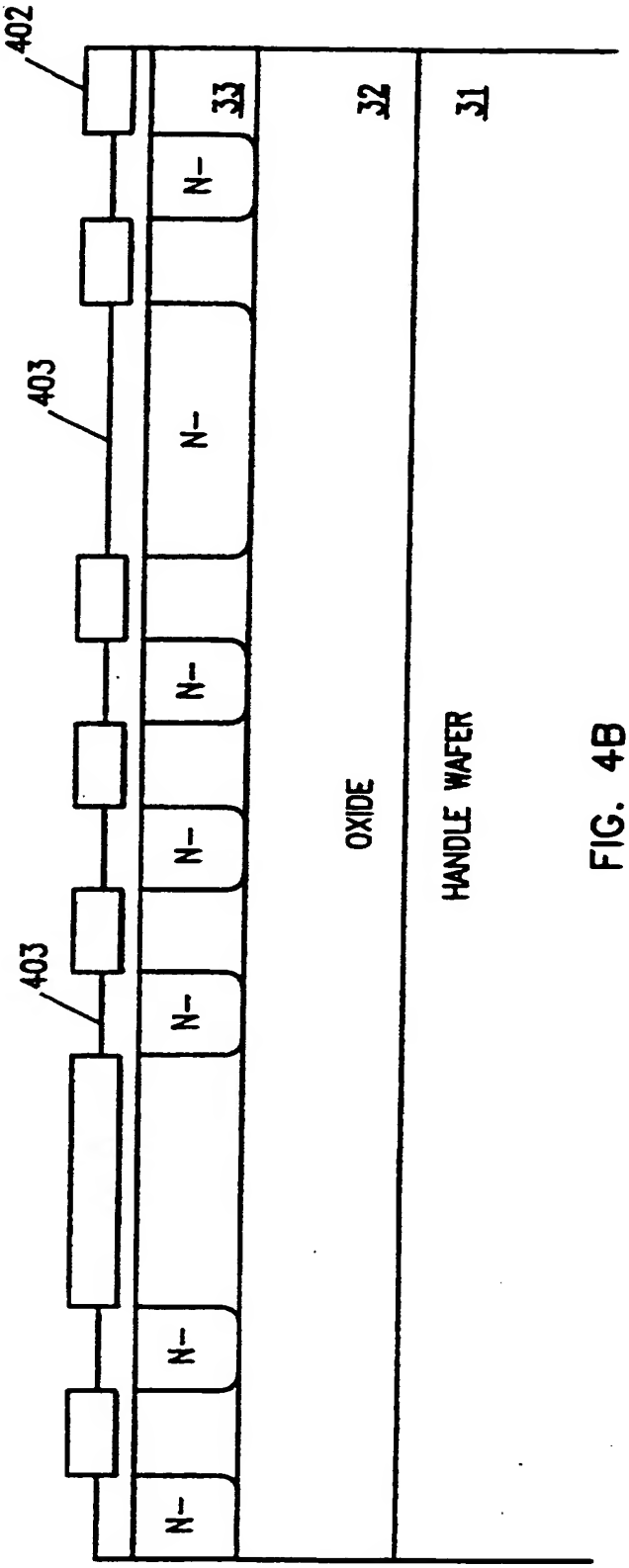


FIG. 4B

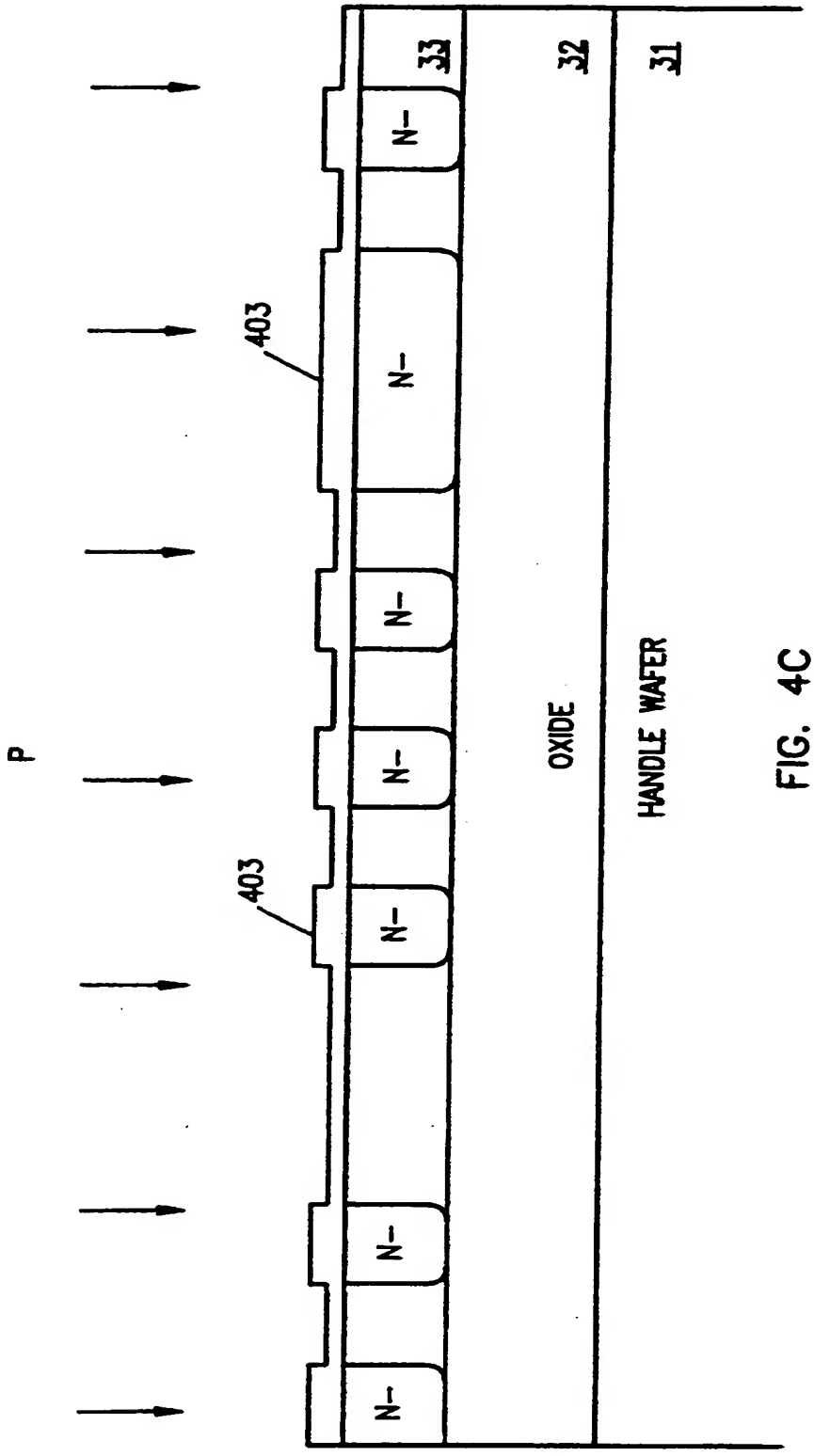


FIG. 4C

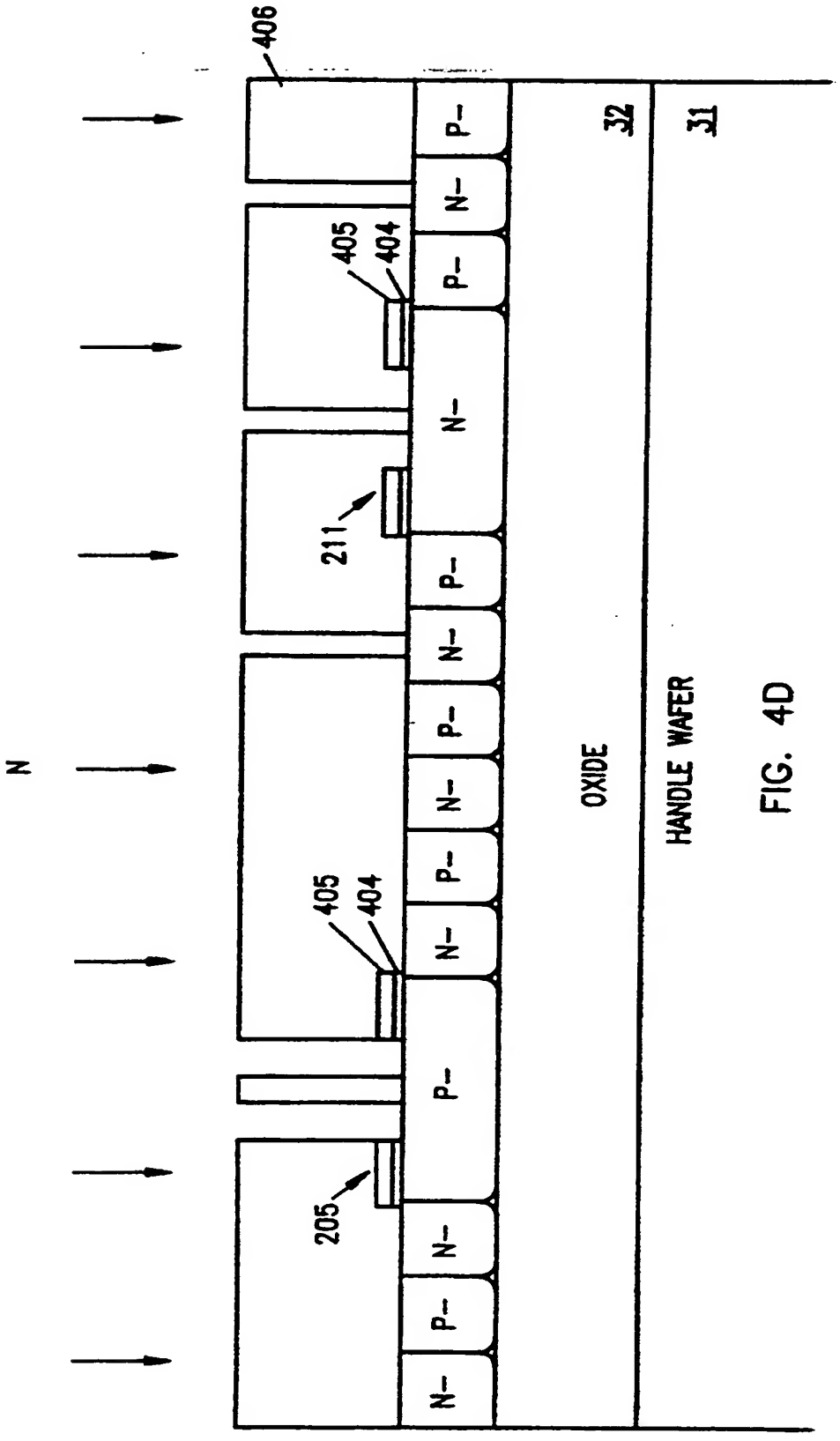


FIG. 4D

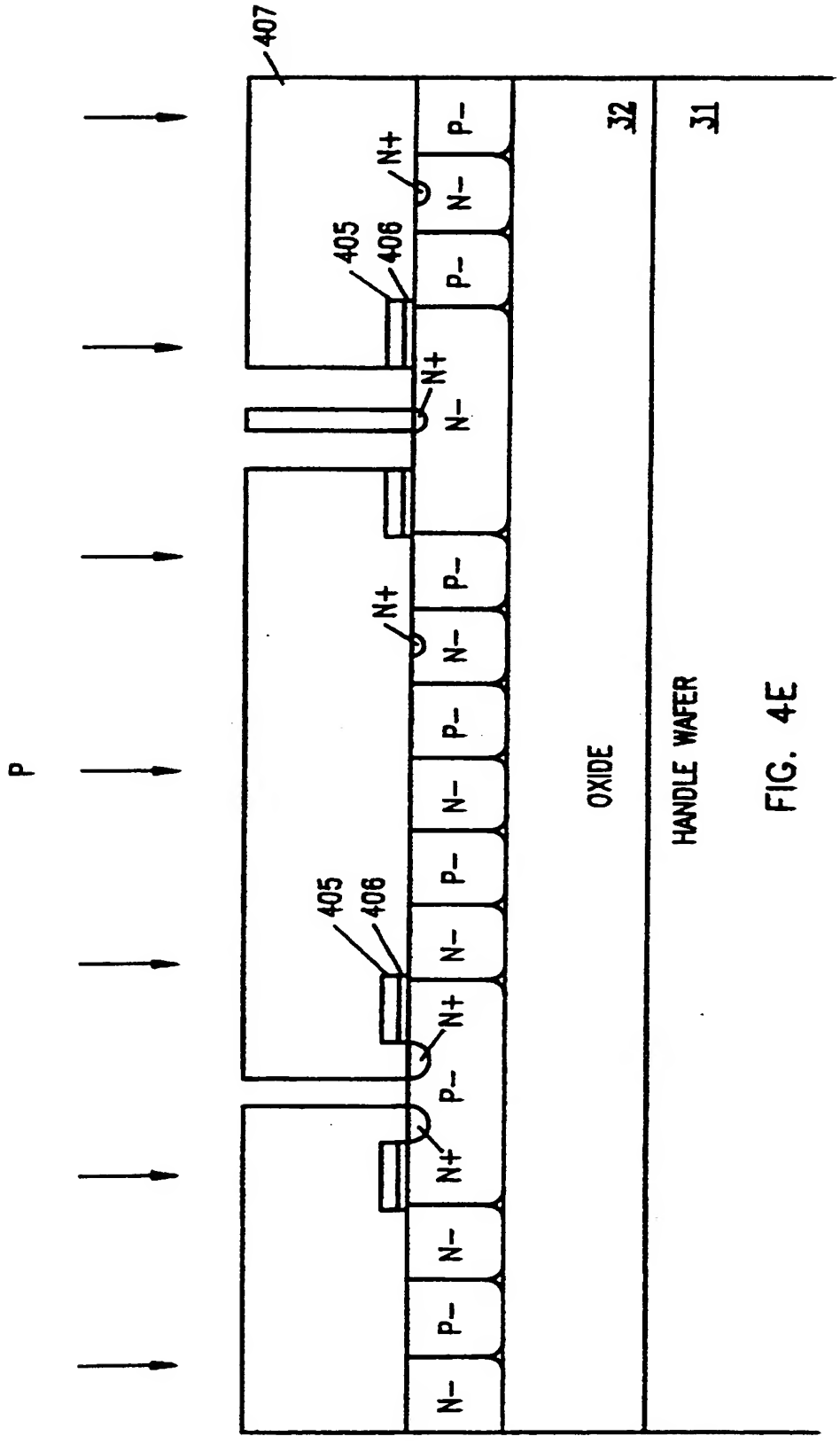


FIG. 4E

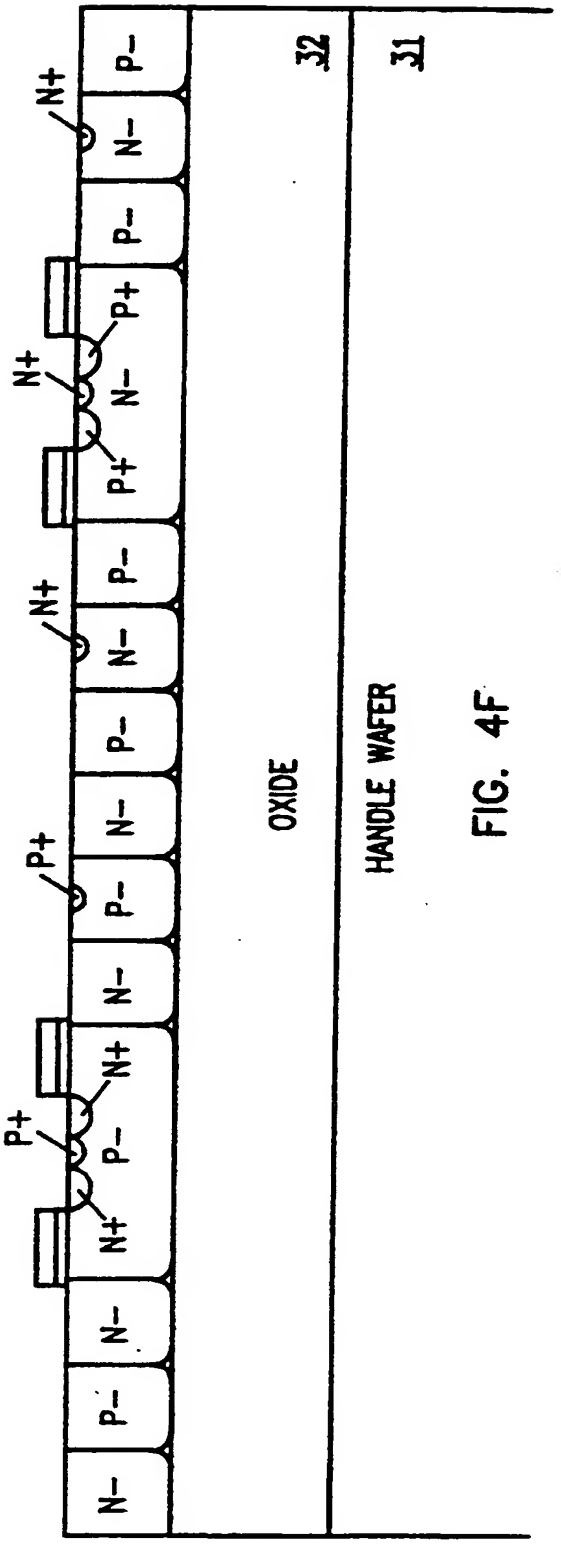


FIG. 4F

INTERNATIONAL SEARCH REPORT

Inter al Application No
PCT/US 96/04620

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L27/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 304 811 (ASEA BROWN BOVERI) 1 March 1989 see page 4, column 6, line 26 - page 5, column 7, line 5; claims 1,4; figures 6-7A	1,8
A	US,A,4 253 162 (HOLLINGSWORTH RICHARD J) 24 February 1981 see column 6, line 49 - column 7, line 35; claims 7-9,11-14; figures 5,6A-6B	1-4
A	US,A,4 918 498 (PLUS DORA ET AL) 17 April 1990 see column 5, line 6 - column 5, line 43 see column 7, line 51 - column 7, line 63; figures 2A-2C	1-3

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
4 July 1996	17. 07. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Fransen, L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter nal Application No
PCT/US 96/04620

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0304811	01-03-89	SE-B-	461490	19-02-90
		DE-A-	3881304	01-07-93
		DE-T-	3881304	16-12-93
		JP-A-	1068970	15-03-89
		SE-A-	8703269	25-02-89
		US-A-	4969023	06-11-90
US-A-4253162	24-02-81	NONE		
US-A-4918498	17-04-90	NONE		